NMOSFETs 91P and 92P and the P-type layers 21P and 22P from each other.

Please replace the paragraph on page 14, beginning on line 9 as follows:

In particular, the semiconductor device 1 has the area AR3 extending over the adjacent areas AR1 and AR2 with the minimum distance. The area AR3 includes areas overlapping with the areas AR1 and AR2 respectively, and the P wells 11 and 12 are partially arranged in the area AR3. A conductive layer (or first conductive layer) 20 is formed in the surface 50S located in the area AR3 (to extend) over the P wells 11 and 12. In more detail, the conductive layer 20, having an end provided on the P well 11 and another end provided on the P well 12, electrically connects the P wells 11 and 12 with each other.

Please replace the paragraph on page 18 beginning on line 20 as follows:

In addition to or in place of the NMOSFETs 91 and 92, memory cells of a DRAM (dynamic random access memory) or an EEPROM (electrically erasable and programmable read only memory) may be formed in the areas AR1 and AR2. In this case, a step of forming memory capacitors is added. A plurality of wiring layers are formed at need for completing an LSI.

Please replace the paragraph on page 19, beginning on line 13 as follows:

Further, according to the semiconductor device 1, P-type layers 21P and 22P and contacts 31P and 32P may not be provided for P wells 11P and 12P dissimilarly to the conventional semiconductor device 1P (see Fig. 22). In addition, the P-type layer 20 is provided in the area AR3 to connect the adjacent P wells 11 and 12 with the minimum distance without providing the conventional element isolation film 51BP. Therefore, the layout area for the P-type layer 20, the contacts 31 and 32 and the wire 40 can be reduced as compared with the conventional semiconductor device 1P. Thus, the overall size of the

semiconductor device (or chip) 1 can be reduced. Consequently, the number of semiconductor devices obtainable from a unit wafer is increased so that the cost can be reduced.

Please replace the paragraph on page 21, beginning on line 9 as follows:

Only a contact 32 may be provided in place of the contact 31. In this case, the contact 32 corresponds to "first contact", the P well 12 corresponds to "first well" and the P well 11 corresponds to "second well".

Please replace the paragraph on page 24, beginning on line 4 as follows:

While the silicon layer 20a is entirely formed deeper than the silicide layer 20b from the surface 50S here, the silicon layer 20a may be formed to enclose the silicide layer 20b in the surface 50S, i.e., the silicide layer 20b may be formed in the silicon layer 20a. In the semiconductor device 4, a contact 33 is arranged in contact with the silicide layer 20b of the conductive layer 21B.

IN THE CLAIMS

Please amend Claims 1 and 5 as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first well of a prescribed conductivity type at which a first semiconductor element is provided, said first well being selectively formed in a surface of said semiconductor substrate;

a second well of the same conductivity type as said prescribed conductivity type at which a second semiconductor element is provided, said second well being selectively formed in said surface of said semiconductor substrate;

a first conductive layer across said first well and said second well in said surface of said semiconductor substrate with an end provided on said first well and another end provided